COMPOSITE SEMICONDUCTOR STRUCTURE
AND DEVICE WITH OPTICAL TESTING ELEMENTS

5   FIELD OF THE INVENTION
     This invention relates generally to semiconductor
structures and devices, and more particularly to
semiconductor structures and devices each of which is a
composite of a monocrystalline noncompound semiconductor
10   material and a monocrystalline compound semiconductor
material, in which the noncompound semiconductor material
contains functional circuitry, and the compound
semiconductor material may contain functional circuitry
and also contains optical testing elements for on-board
15   testing and for coupling on-board testing structures or
circuits to external testing equipment.

          BACKGROUND OF THE INVENTION
     The vast majority of semiconductor integrated
20   circuits are fabricated from silicon, at least in part
because of the availability of inexpensive, high quality
monocrystalline silicon substrates. For testing
purposes, such integrated circuits are normally
fabricated with circuit elements whose sole purpose is to

allow verification that the fabrication process proceeded as intended.

For example, one typical testing structure or circuit includes a chain or chains of registers that have no intended use in the final device, although components that may have an intended subsequent use can also be included. After fabrication is complete, a predetermined pattern of signals is propagated or "scanned" through the chain or chains--typically referred to as "scan chains"-- and the pattern of signals output by each scan chain is compared to pattern of signals input into each scan chain. If the output patterns are the patterns expected based on the input patterns, then one may assume with some acceptable degree of confidence that each component in the scan chain operated correctly and therefore was fabricated correctly. One further assumes that components neighboring each scan chain component also were fabricated correctly and therefore that the complete device is acceptable.

If the output patterns deviate from what is expected, one may assume that there is a defect caused by improper fabrication. In that case, the entire device may be discarded, or it may be possible to isolate the problem area of the device and, if that area is not too large, use the remainder of the device. One way to isolate the defective area may be to confine each scan chain to an identifiable portion of the device, so that for each chain that does not correctly propagate the test signal, the area to be examined to isolate the defect is limited to the area traversed by that scan chain. In order to further isolate the defective area, it may be necessary to probe intermediate points along that scan

chain, in order to see where the propagated signal begins to deviate from the expected signal.

Scan chains have certain limitations. First, one must make assumptions based on scan results about
5 portions of the semiconductor device that themselves were not scanned. In addition, typically, there is more than one scan chain in each integrated circuit device, and intermediate probe points, as discussed above, may be provided along the scan chains. In a large integrated
10 circuit device, the total number of probe points, including the end points of each scan chain and the intermediate points, if any, can number several hundred. Known testing equipment uses mechanical probes to contact pads provided for that purpose, some or all of which may
15 be the wire bond pads to be used in the intended use of the device. Each of those probes must be properly aligned and must contact its respective pad with substantially identical pressure to assure accurate test results.
20 Thus a need exists for a semiconductor integrated circuit device in which circuit elements can be tested directly. A need also exists for a semiconductor integrated circuit device that can be tested with reduced reliance on the use of mechanical probes.

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BRIEF DESCRIPTION OF THE DRAWINGS

FIGs. 1, 2, 3, 24, 25 illustrate schematically, in cross section, device structures that can be used in accordance with various embodiments of the invention.
30 FIG. 4 illustrates graphically the relationship between maximum attainable film thickness and lattice mismatch between a host crystal and a grown crystalline overlayer.

FIG. 5 is a high resolution Transmission Electron Micrograph (TEM) of illustrative semiconductor material manufactured in accordance with what is shown herein.

FIG. 6 is an x-ray diffraction taken on an illustrative semiconductor structure manufactured in accordance with what is shown herein.

FIG. 7 illustrates a high resolution Transmission Electron Micrograph of a structure including an amorphous oxide layer.

FIG. 8 illustrates an x-ray diffraction spectrum of a structure including an amorphous oxide layer.

FIGs. 9-12 illustrate schematically, in cross-section, the formation of a device structure in accordance with another embodiment of the invention.

FIGs. 13-16 illustrate a probable molecular bonding structure of the device structures illustrated in FIGs. 9-12.

FIGs. 17-20 illustrate schematically, in cross-section, the formation of a device structure in accordance with still another embodiment of the invention.

FIGs. 21-23 illustrate schematically, in cross section, the formation of a yet another embodiment of a device structure in accordance with the invention.

FIGs. 26-30 include illustrations of cross-sectional views of a portion of an integrated circuit that includes a compound semiconductor portion, a bipolar portion, and a MOS portion in accordance with what is shown herein.

FIGs. 31-37 include illustrations of cross-sectional views of a portion of another integrated circuit that includes a semiconductor laser and a MOS transistor in accordance with what is shown herein.

FIGs. 38 and 39 show a cross-sectional and a plan view, respectively, of a hybrid semiconductor structure including compound semiconductor islands in a silicon substrate.

5   FIG. 40 shows an intermediate step in the formation of the hybrid structure of FIGs. 38 and 39.

FIG. 41 shows a further optional processing step in the formation of the hybrid structure of FIGs. 31 and 32.

FIG. 42 shows a cross-sectional view of a portion of

10   an integrated circuit that includes a compound semiconductor portion and an MOS portion in accordance with what is shown herein.

FIG. 43 shows a schematic plan view of an integrated circuit chip incorporating a first aspect of the present

15   invention.

FIG. 44 shows a fragmentary schematic perspective view of a testing apparatus in accordance with the first aspect of the present invention.

FIG. 45 shows a schematic cross-sectional view of

20   some of the elements of FIG. 44.

FIGs. 46 and 47 each show a schematic cross-sectional view of an integrated circuit chip incorporating a second aspect of the present invention.

Skilled artisans will appreciate that in many cases

25   elements in certain FIGs. are illustrated for simplicity and clarity and have not necessarily been drawn to scale. For example, the dimensions of some of the elements in certain FIGs. may be exaggerated relative to other elements to help to improve understanding of what is

30   being shown.

DETAILED DESCRIPTION OF THE DRAWINGS

The present invention involves semiconductor structures of particular types. For convenience herein, these semiconductor structures are sometimes referred to
5   as "composite semiconductor structures" or "composite integrated circuits" because they include two (or more) significantly different types of semiconductor devices in one integrated structure or circuit. For example, one of these two types of devices may be silicon-based devices
10 such as CMOS devices, and the other of these two types of devices may be compound semiconductor devices such GaAs devices. Illustrative composite semiconductor structures and methods for making such structures are disclosed in Ramdani et al. U.S. patent application No. 09/502,023,
15 filed February 10, 2000, which is hereby incorporated by reference herein in its entirety. Certain material from that reference is substantially repeated below to ensure that there is support herein for references to composite semiconductor structures and composite integrated
20 circuits.

FIG. 1 illustrates schematically, in cross section, a portion of a semiconductor structure 20 which may be relevant to or useful in connection with certain embodiments of the present invention. Semiconductor
25 structure 20 includes a monocrystalline substrate 22, accommodating buffer layer 24 comprising a monocrystalline material, and a layer 26 of a monocrystalline compound semiconductor material. In this context, the term "monocrystalline" shall have the
30 meaning commonly used within the semiconductor industry. The term shall refer to materials that are a single crystal or that are substantially a single crystal and shall include those materials having a relatively small

number of defects such as dislocations and the like as
are commonly found in substrates of silicon or germanium
or mixtures of silicon and germanium and epitaxial layers
of such materials commonly found in the semiconductor

5   industry.

In accordance with one embodiment, structure 20 also
includes an amorphous intermediate layer 28 positioned
between substrate 22 and accommodating buffer layer 24.
Structure 20 may also include a template layer 30 between

10 accommodating buffer layer 24 and compound semiconductor
layer 26. As will be explained more fully below,
template layer 30 helps to initiate the growth of
compound semiconductor layer 26 on accommodating buffer
layer 24. Amorphous intermediate layer 28 helps to

15 relieve the strain in accommodating buffer layer 24 and
by doing so, aids in the growth of a high crystalline
quality accommodating buffer layer 24.

Substrate 22, in accordance with one embodiment, is
a monocrystalline semiconductor wafer, preferably of

20 large diameter. The wafer can be of a material from
Group IV of the periodic table, and preferably a material
from Group IVB, e.g., Carbon, Silicon, etc. Examples of
Group IV semiconductor materials include silicon,
germanium, mixed silicon and germanium, mixed silicon and

25 carbon, mixed silicon, germanium and carbon, and the
like. Preferably substrate 22 is a wafer containing
silicon or germanium, and most preferably is a high
quality monocrystalline silicon wafer as used in the
semiconductor industry. Accommodating buffer layer 24 is

30 preferably a monocrystalline oxide or nitride material
epitaxially grown on the underlying substrate 22. In
accordance with one embodiment, amorphous intermediate
layer 28 is grown on substrate 22 at the interface

between substrate 22 and the growing accommodating buffer layer 24 by the oxidation of substrate 22 during the growth of layer 24. Amorphous intermediate layer 28 serves to relieve strain that might otherwise occur in

5   monocrystalline accommodating buffer layer 24 as a result of differences in the lattice constants of substrate 22 and buffer layer 24. As used herein, lattice constant refers to the distance between atoms of a cell measured in the plane of the surface. If such strain is not

10   relieved by amorphous intermediate layer 28, the strain may cause defects in the crystalline structure of accommodating buffer layer 24. Defects in the crystalline structure of accommodating buffer layer 24, in turn, would make it difficult to achieve a high

15   quality crystalline structure in monocrystalline compound semiconductor layer 26.

     Accommodating buffer layer 24 is preferably a monocrystalline oxide or nitride material selected for its crystalline compatibility with underlying substrate

20   22 and with overlying compound semiconductor material 26. For example, the material could be an oxide or nitride having a lattice structure matched to substrate 22 and to the subsequently applied semiconductor material 26. Materials that are suitable for accommodating buffer

25   layer 24 include metal oxides such as the alkaline earth metal titanates, alkaline earth metal zirconates, alkaline earth metal hafnates, alkaline earth metal tantalates, alkaline earth metal ruthenates, alkaline earth metal niobates, alkaline earth metal vanadates,

30   alkaline earth metal tin-based perovskites, lanthanum aluminate, lanthanum scandium oxide, and gadolinium oxide. Additionally, various nitrides such as gallium nitride, aluminum nitride, and boron nitride may also be

used for accommodating buffer layer 24. Most of these
materials are insulators, although strontium ruthenate,
for example, is a conductor. Generally, these materials
are metal oxides or metal nitrides, and more

5 particularly, these metal oxide or nitrides typically
include at least two different metallic elements. In
some specific applications, the metal oxides or nitride
may include three or more different metallic elements.

Amorphous interface layer 28 is preferably an oxide

10 formed by the oxidation of the surface of substrate 22,
and more preferably is composed of a silicon oxide. The
thickness of layer 28 is sufficient to relieve strain
attributed to mismatches between the lattice constants of
substrate 22 and accommodating buffer layer 24.

15 Typically, layer 28 has a thickness in the range of
approximately 0.5-5 nm.

The compound semiconductor material of layer 26 can
be selected, as needed for a particular semiconductor
structure, from any of the Group IIIA and VA elements

20 (III-V semiconductor compounds), mixed III-V compounds,
Group II(A or B) and VIA elements (II-VI semiconductor
compounds), and mixed II-VI compounds. Examples include
gallium arsenide (GaAs), gallium indium arsenide
(GaInAs), gallium aluminum arsenide (GaAlAs), indium

25 phosphide (InP), cadmium sulfide (CDS), cadmium mercury
telluride (CdHgTe), zinc selenide (ZnSe), zinc sulfur
selenide (ZnSSe), and the like. Suitable template 30
materials chemically bond to the surface of the
accommodating buffer layer 24 at selected sites and

30 provide sites for the nucleation of the epitaxial growth
of the subsequent compound semiconductor layer 26.
Appropriate materials for template 30 are discussed
below.

FIG. 2 illustrates, in cross section, a portion of a semiconductor structure 40 in accordance with a further embodiment. Structure 40 is similar to the previously described semiconductor structure 20 except that an

5   additional buffer layer 32 is positioned between accommodating buffer layer 24 and layer of monocrystalline compound semiconductor material 26. Specifically, additional buffer layer 32 is positioned between the template layer 30 and the overlying layer 26

10   of compound semiconductor material. Additional buffer layer 32, formed of a semiconductor or compound semiconductor material, serves to provide a lattice compensation when the lattice constant of accommodating buffer layer 24 cannot be adequately matched to the

15   overlying monocrystalline compound semiconductor material layer 26.

FIG. 3 schematically illustrates, in cross section, a portion of a semiconductor structure 34 in accordance with another exemplary embodiment of the invention.

20   Structure 34 is similar to structure 20, except that structure 34 includes an amorphous layer 36, rather than accommodating buffer layer 24 and amorphous interface layer 28, and an additional semiconductor layer 38.

As explained in greater detail below, amorphous

25   layer 36 may be formed by first forming an accommodating buffer layer and an amorphous interface layer in a similar manner to that described above. Monocrystalline semiconductor layer 26 is then formed (by epitaxial growth) overlying the monocrystalline accommodating

30   buffer layer. The accommodating buffer layer is then exposed to an anneal process to convert the monocrystalline accommodating buffer layer to an amorphous layer. Amorphous layer 36 formed in this

manner comprises materials from both the accommodating
buffer and interface layers, which amorphous layers may
or may not amalgamate. Thus, layer 36 may comprise one
or two amorphous layers. Formation of amorphous layer 36

5 between substrate 22 and semiconductor layer 38
(subsequent to layer 38 formation) relieves stresses
between layers 22 and 38 and provides a true compliant
substrate for subsequent processing--*e.g.*, compound
semiconductor layer 26 formation.

10 The processes previously described above in
connection with FIGS. 1 and 2 are adequate for growing
monocrystalline compound semiconductor layers over a
monocrystalline substrate. However, the process
described in connection with FIG. 3, which includes

15 transforming a monocrystalline accommodating buffer layer
to an amorphous oxide layer, may be better for growing
monocrystalline compound semiconductor layers because it
allows any strain in layer 26 to relax.

Semiconductor layer 38 may include any of the

20 materials described throughout this application in
connection with either of compound semiconductor material
layer 26 or additional buffer layer 32. For example,
layer 38 may include monocrystalline Group IV or
monocrystalline compound semiconductor materials.

25 In accordance with one embodiment of the present
invention, semiconductor layer 38 serves as an anneal cap
during layer 36 formation and as a template for
subsequent semiconductor layer 26 formation.
Accordingly, layer 38 is preferably thick enough to

30 provide a suitable template for layer 26 growth (at least
one monolayer) and thin enough to allow layer 38 to form
as a substantially defect free monocrystalline
semiconductor compound.

In accordance with another embodiment of the invention, semiconductor layer 38 comprises compound semiconductor material (*e.g.*, a material discussed above in connection with compound semiconductor layer 26) that

5 is thick enough to form devices within layer 38. In this case, a semiconductor structure in accordance with the present invention does not include compound semiconductor layer 26. In other words, the semiconductor structure in accordance with this embodiment only includes one

10 compound semiconductor layer disposed above amorphous oxide layer 36.

The layer formed on substrate 22, whether it includes only accommodating buffer layer 24, accommodating buffer layer 24 with amorphous intermediate

15 or interface layer 28, or an amorphous layer such as layer 36 formed by annealing layers 24 and 28 as described above in connection with FIG. 3, may be referred to generically as an "accommodating layer."

The following non-limiting, illustrative examples

20 illustrate various combinations of materials useful in structures 20, 40 and 34 in accordance with various alternative embodiments. These examples are merely illustrative, and it is not intended that the invention be limited to these illustrative examples.

25

Example 1

In accordance with one embodiment, monocrystalline substrate 22 is a silicon substrate oriented in the (100) direction. Silicon substrate 22 can be, for example, a

30 silicon substrate as is commonly used in making complementary metal oxide semiconductor (CMOS) integrated circuits having a diameter of about 200-300 mm. In accordance with this embodiment, accommodating buffer

layer 24 is a monocrystalline layer of $Sr_zBa_{1-z}TiO_3$ where z ranges from 0 to 1 and amorphous intermediate layer 28 is a layer of silicon oxide (SiO_x) formed at the interface between silicon substrate 22 and accommodating buffer

5   layer 24. The value of z is selected to obtain one or more lattice constants closely matched to corresponding lattice constants of the subsequently formed layer 26. Accommodating buffer layer 24 can have a thickness of about 2 to about 100 nanometers (nm) and preferably has a

10 thickness of about 10 nm. In general, it is desired to have an accommodating buffer layer 24 thick enough to isolate monocrystalline material layer 26 from substrate 22 to obtain the desired electrical and optical properties. Layers thicker than 100 nm usually provide

15 little additional benefit while increasing cost unnecessarily; however, thicker layers may be fabricated if needed. The amorphous intermediate layer 28 of silicon oxide can have a thickness of about 0.5-5 nm, and preferably a thickness of about 1.5-2.5 nm.

20   In accordance with this embodiment, compound semiconductor material layer 26 is a layer of gallium arsenide (GaAs) or aluminum gallium arsenide (AlGaAs) having a thickness of about 1 nm to about 100 micrometers (μm) and preferably a thickness of about 0.5 μm to 10 μm.

25 The thickness generally depends on the application for which the layer is being prepared. To facilitate the epitaxial growth of the gallium arsenide or aluminum gallium arsenide on the monocrystalline oxide, a template layer 30 is formed by capping the oxide layer. Template

30 layer 30 is preferably 1-10 monolayers of Ti-As, Sr-O-As, Sr-Ga-O, or Sr-Al-O. By way of a preferred example, 1-2 monolayers 30 of Ti-As or Sr-Ga-O have been shown to successfully grow GaAs layers 26.

Example 2

In accordance with a further embodiment, monocrystalline substrate 22 is a silicon substrate as

5   described above. Accommodating buffer layer 24 is a monocrystalline oxide of strontium or barium zirconate or hafnate in a cubic or orthorhombic phase with an amorphous intermediate layer 28 of silicon oxide formed at the interface between silicon substrate 22 and

10 accommodating buffer layer 24. Accommodating buffer layer 24 can have a thickness of about 2-100 nm and preferably has a thickness of at least 5 nm to ensure adequate crystalline and surface quality and is formed of a monocrystalline $SrZrO_3$, $BaZrO_3$, $SrHfO_3$, $BaSnO_3$ or $BaHfO_3$.

15 For example, a monocrystalline oxide layer of $BaZrO_3$ can grow at a temperature of about 700 degrees C. The lattice structure of the resulting crystalline oxide exhibits a 45 degree rotation with respect to the substrate 22 silicon lattice structure.

20   An accommodating buffer layer 24 formed of these zirconate or hafnate materials is suitable for the growth of compound semiconductor materials 26 in the indium phosphide (InP) system. The compound semiconductor material 26 can be, for example, indium phosphide (InP),

25 indium gallium arsenide (InGaAs), aluminum indium arsenide, (AlInAs), or aluminum gallium indium arsenic phosphide (AlGaInAsP), having a thickness of about 1.0 nm to 10 µm. A suitable template 30 for this structure is 1-10 monolayers of zirconium-arsenic (Zr-As), zirconium-

30 phosphorus (Zr-P), hafnium-arsenic (Hf-As), hafnium-phosphorus (Hf-P), strontium-oxygen-arsenic (Sr-O-As), strontium-oxygen-phosphorus (Sr-O-P), barium-oxygen-arsenic (Ba-O-As), indium-strontium-oxygen (In-Sr-O), or

barium-oxygen-phosphorus (Ba-O-P), and preferably 1-2

monolayers of one of these materials. By way of an

example, for a barium zirconate accommodating buffer

layer 24, the surface is terminated with 1-2 monolayers

5   of zirconium followed by deposition of 1-2 monolayers of

arsenic to form a Zr-As template 30. A monocrystalline

layer 26 of the compound semiconductor material from the

indium phosphide system is then grown on template layer

30. The resulting lattice structure of the compound

10   semiconductor material 26 exhibits a 45 degree rotation

with respect to the accommodating buffer layer 24 lattice

structure and a lattice mismatch to (100) InP of less

than 2.5%, and preferably less than about 1.0%.

15   Example 3

    In accordance with a further embodiment, a structure

is provided that is suitable for the growth of an

epitaxial film of a II-VI material overlying a silicon

substrate 22. The substrate 22 is preferably a silicon

20   wafer as described above. A suitable accommodating

buffer layer 24 material is $Sr_xBa_{1-x}TiO_3$, where x ranges

from 0 to 1, having a thickness of about 2-100 nm and

preferably a thickness of about 5-15 nm. The II-VI

compound semiconductor material 26 can be, for example,

25   zinc selenide (ZnSe) or zinc sulfur selenide (ZnSSe). A

suitable template 30 for this material system includes 1-

10 monolayers of zinc-oxygen (Zn-O) followed by 1-2

monolayers of an excess of zinc followed by the

selenidation of zinc on the surface. Alternatively, a

30   template 30 can be, for example, 1-10 monolayers of

strontium-sulfur (Sr-S) followed by the ZnSeS.

Example 4

This embodiment of the invention is an example of
structure 40 illustrated in FIG. 2. Substrate 22,
monocrystalline oxide layer 24, and monocrystalline

5   compound semiconductor material layer 26 can be similar
to those described in example 1. In addition, an
additional buffer layer 32 serves to alleviate any
strains that might result from a mismatch of the crystal
lattice of the accommodating buffer layer and the lattice

10   of the monocrystalline semiconductor material. The
additional buffer layer 32 can be a layer of germanium or
a GaAs, an aluminum gallium arsenide (AlGaAs), an indium
gallium phosphide (InGaP), an aluminum gallium phosphide
(AlGaP), an indium gallium arsenide (InGaAs), an aluminum

15   indium phosphide (AlInP), a gallium arsenide phosphide
(GaAsP), or an indium gallium phosphide (InGaP) strain
compensated superlattice. In accordance with one aspect
of this embodiment, buffer layer 32 includes a $GaAs_xP_{1-x}$
superlattice, wherein the value of x ranges from 0 to 1.

20   In accordance with another aspect, buffer layer 32
includes an $In_yGa_{1-y}P$ superlattice, wherein the value of y
ranges from 0 to 1. By varying the value of x or y, as
the case may be, the lattice constant is varied from
bottom to top across the superlattice to create a match

25   between lattice constants of the underlying oxide and the
overlying compound semiconductor material. The
compositions of other materials, such as those listed
above, may also be similarly varied to manipulate the
lattice constant of layer 32 in a like manner. The

30   superlattice can have a thickness of about 50-500 nm and
preferably has a thickness of about 100-200 nm. The
template for this structure can be the same of that
described in example 1. Alternatively, buffer layer 32

can be a layer of monocrystalline germanium having a
thickness of 1-50 nm and preferably having a thickness of
about 2-20 nm. In using a germanium buffer layer, a
template layer of either germanium-strontium (Ge-Sr) or

5 germanium-titanium (Ge-Ti) having a thickness of about
one monolayer can be used as a nucleating site for the
subsequent growth of the monocrystalline compound
semiconductor material layer. The formation of the oxide
layer is capped with either a monolayer of strontium or a

10 monolayer of titanium to act as a nucleating site for the
subsequent deposition of the monocrystalline germanium.
The monolayer of strontium or titanium provides a
nucleating site to which the first monolayer of germanium
can bond.

15

                          Example 5
    This example also illustrates materials useful in a
structure 40 as illustrated in FIG. 2. Substrate
material 22, accommodating buffer layer 24,

20 monocrystalline compound semiconductor material layer 26
and template layer 30 can be the same as those described
above in example 2. In addition, a buffer layer 32 is
inserted between accommodating buffer layer 24 and
overlying monocrystalline compound semiconductor material

25 layer 26. Buffer layer 32, a further monocrystalline
semiconductor material, can be, for example, a graded
layer of indium gallium arsenide (InGaAs) or indium
aluminum arsenide (InAlAs). In accordance with one
aspect of this embodiment, buffer layer 32 includes

30 InGaAs, in which the indium composition varies from 0 to
about 47%. The additional buffer layer 32 preferably has
a thickness of about 10-30 nm. Varying the composition
of buffer layer 32 from GaAs to InGaAs serves to provide

a lattice match between the underlying monocrystalline
oxide material 24 and the overlying layer 26 of
monocrystalline compound semiconductor material. Such a
buffer layer 32 is especially advantageous if there is a
5   lattice mismatch between accommodating buffer layer 24
and monocrystalline compound semiconductor material layer
26.

Example 6
10   This example provides exemplary materials useful in
structure 34, as illustrated in FIG. 3. Substrate
material 22, template layer 30, and monocrystalline
compound semiconductor material layer 26 may be the same
as those described above in connection with example 1.
15   Amorphous layer 36 is an amorphous oxide layer which
is suitably formed of a combination of amorphous
intermediate layer materials (e.g., layer 28 materials as
described above) and accommodating buffer layer materials
(e.g., layer 24 materials as described above). For
20   example, amorphous layer 36 may include a combination of
SiO_x and $Sr_zBa_{1-z}TiO_3$ (where z ranges from 0 to 1),which
combine or mix, at least partially, during an anneal
process to form amorphous oxide layer 36.
The thickness of amorphous layer 36 may vary from
25   application to application and may depend on such factors
as desired insulating properties of layer 36, type of
semiconductor material comprising layer 26, and the like.
In accordance with one exemplary aspect of the present
embodiment, layer 36 thickness is about 2 nm to about 100
30   nm, preferably about 2-10 nm, and more preferably about
5-6 nm.
Layer 38 comprises a monocrystalline compound
semiconductor material that can be grown epitaxially over

a monocrystalline oxide material such as material used to form accommodating buffer layer 24. In accordance with one embodiment of the invention, layer 38 includes the same materials as those comprising layer 26. For

5   example, if layer 26 includes GaAs, layer 38 also includes GaAs. However, in accordance with other embodiments of the present invention, layer 38 may include materials different from those used to form layer 26. In accordance with one exemplary embodiment of the

10   invention, layer 38 is about 1 monolayer to about 100 nm thick.

Referring again to FIGS. 1-3, substrate 22 is a monocrystalline substrate such as a monocrystalline silicon substrate. The crystalline structure of the

15   monocrystalline substrate is characterized by a lattice constant and by a lattice orientation. In similar manner, accommodating buffer layer 24 is also a monocrystalline material and the lattice of that monocrystalline material is characterized by a lattice

20   constant and a crystal orientation. The lattice constants of accommodating buffer layer 24 and monocrystalline substrate 22 must be closely matched or, alternatively, must be such that upon rotation of one crystal orientation with respect to the other crystal

25   orientation, a substantial match in lattice constants is achieved. In this context the terms "substantially equal" and "substantially matched" mean that there is sufficient similarity between the lattice constants to permit the growth of a high quality crystalline layer on

30   the underlying layer.

FIG. 4 illustrates graphically the relationship of the achievable thickness of a grown crystal layer of high crystalline quality as a function of the mismatch between

the lattice constants of the host crystal and the grown crystal. Curve 42 illustrates the boundary of high crystalline quality material. The area to the right of curve 42 represents layers that tend to be

5   polycrystalline. With no lattice mismatch, it is theoretically possible to grow an infinitely thick, high quality epitaxial layer on the host crystal. As the mismatch in lattice constants increases, the thickness of achievable, high quality crystalline layer decreases

10   rapidly. As a reference point, for example, if the lattice constants between the host crystal and the grown layer are mismatched by more than about 2%, monocrystalline epitaxial layers in excess of about 20 nm cannot be achieved.

15   In accordance with one embodiment, substrate 22 is a (100) or (111) oriented monocrystalline silicon wafer and accommodating buffer layer 24 is a layer of strontium barium titanate. Substantial matching of lattice constants between these two materials is achieved by

20   rotating the crystal orientation of the titanate material 24 by 45° with respect to the crystal orientation of the silicon substrate wafer 22. The inclusion in the structure of amorphous interface layer 28, a silicon oxide layer in this example, if it is of sufficient

25   thickness, serves to reduce strain in the titanate monocrystalline layer 24 that might result from any mismatch in the lattice constants of the host silicon wafer 22 and the grown titanate layer 24. As a result, a high quality, thick, monocrystalline titanate layer 24 is

30   achievable.

         Still referring to FIGS. 1-3, layer 26 is a layer of epitaxially grown monocrystalline material and that crystalline material is also characterized by a crystal

lattice constant and a crystal orientation. In

accordance with one embodiment of the invention, the

lattice constant of layer 26 differs from the lattice

constant of substrate 22. To achieve high crystalline

5 quality in this epitaxially grown monocrystalline layer,

accommodating buffer layer 24 must be of high crystalline

quality. In addition, in order to achieve high

crystalline quality in layer 26, substantial matching

between the crystal lattice constant of the host crystal,

10 in this case, monocrystalline accommodating buffer layer

24, and grown crystal 26 is desired. With properly

selected materials this substantial matching of lattice

constants is achieved as a result of rotation of the

crystal orientation of grown crystal 26 with respect to

15 the orientation of host crystal 24. If grown crystal 26

is gallium arsenide, aluminum gallium arsenide, zinc

selenide, or zinc sulfur selenide and accommodating

buffer layer 24 is monocrystalline $Sr_xBa_{1-x}TiO_3$,

substantial matching of crystal lattice constants of the

20 two materials is achieved, wherein the crystal

orientation of grown layer 26 is rotated by 45° with

respect to the orientation of the host monocrystalline

oxide 24. Similarly, if host material 24 is a strontium

or barium zirconate or a strontium or barium hafnate or

25 barium tin oxide and compound semiconductor layer 26 is

indium phosphide or gallium indium arsenide or aluminum

indium arsenide, substantial matching of crystal lattice

constants can be achieved by rotating the orientation of

grown crystal layer 26 by 45° with respect to host oxide

30 crystal 24. In some instances, a crystalline

semiconductor buffer layer 32 between host oxide 24 and

grown compound semiconductor layer 26 can be used to

reduce strain in grown monocrystalline compound
semiconductor layer 26 that might result from small
differences in lattice constants.   Better crystalline
quality in grown monocrystalline compound semiconductor
5   layer 26 can thereby be achieved.

The following example illustrates a process, in
accordance with one embodiment, for fabricating a
semiconductor structure such as the structures depicted
in FIGS. 1-3.   The process starts by providing a
10   monocrystalline semiconductor substrate 22 comprising
silicon or germanium.   In accordance with a preferred
embodiment, semiconductor substrate 22 is a silicon wafer
having a (100) orientation.   Substrate 22 is preferably
oriented on axis or, at most, about 0.5° off axis.   At
15   least a portion of semiconductor substrate 22 has a bare
surface, although other portions of the substrate, as
described below, may encompass other structures.   The
term "bare" in this context means that the surface in the
portion of substrate 22 has been cleaned to remove any
20   oxides, contaminants, or other foreign material.   As is
well known, bare silicon is highly reactive and readily
forms a native oxide.   The term "bare" is intended to
encompass such a native oxide.   A thin silicon oxide may
also be intentionally grown on the semiconductor
25   substrate, although such a grown oxide is not essential
to the process.   In order to epitaxially grow a
monocrystalline oxide layer 24 overlying monocrystalline
substrate 22, the native oxide layer must first be
removed to expose the crystalline structure of underlying
30   substrate 22.   The following process is preferably
carried out by molecular beam epitaxy (MBE), although
other epitaxial processes may also be used in accordance
with the present invention.   The native oxide can be

removed by first thermally depositing a thin layer of
strontium, barium, a combination of strontium and barium,
or other alkaline earth metals or combinations of
alkaline earth metals in an MBE apparatus. In the case
5   where strontium is used, the substrate 22 is then heated
to a temperature of about 850°C to cause the strontium to
react with the native silicon oxide layer. The strontium
serves to reduce the silicon oxide to leave a silicon
oxide-free surface. The resultant surface, which
10 exhibits an ordered 2x1 structure, includes strontium,
oxygen, and silicon. The ordered 2x1 structure forms a
template for the ordered growth of an overlying layer 24
of a monocrystalline oxide. The template provides the
necessary chemical and physical properties to nucleate
15 the crystalline growth of an overlying layer 24.

In accordance with an alternate embodiment, the
native silicon oxide can be converted and the surface of
substrate 22 can be prepared for the growth of a
monocrystalline oxide layer 24 by depositing an alkaline
20 earth metal oxide, such as strontium oxide or barium
oxide, onto the substrate surface by MBE at a low
temperature and by subsequently heating the structure to
a temperature of about 850°C. At this temperature a solid
state reaction takes place between the strontium oxide
25 and the native silicon oxide causing the reduction of the
native silicon oxide and leaving an ordered 2x1 structure
with strontium, oxygen, and silicon remaining on the
substrate 22 surface. Again, this forms a template for
the subsequent growth of an ordered monocrystalline oxide
30 layer 24.

Following the removal of the silicon oxide from the
surface of substrate 22, the substrate is cooled to a

temperature in the range of about 200-800°C and a layer 24 of strontium titanate is grown on the template layer by molecular beam epitaxy. The MBE process is initiated by opening shutters in the MBE apparatus to expose

5   strontium, titanium and oxygen sources. The ratio of strontium and titanium is approximately 1:1. The partial pressure of oxygen is initially set at a minimum value to grow stoichiometric strontium titanate at a growth rate of about 0.3-0.5 nm per minute. After initiating growth

10   of the strontium titanate, the partial pressure of oxygen is increased above the initial minimum value. The overpressure of oxygen causes the growth of an amorphous silicon oxide layer 28 at the interface between underlying substrate 22 and the growing strontium

15   titanate layer 24. The growth of silicon oxide layer 28 results from the diffusion of oxygen through the growing strontium titanate layer 24 to the interface where the oxygen reacts with silicon at the surface of underlying substrate 22. The strontium titanate grows as an ordered

20   (100) monocrystal 24 with the (100) crystalline orientation rotated by 45° with respect to the underlying substrate 22. Strain that otherwise might exist in strontium titanate layer 24 because of the small mismatch in lattice constant between silicon substrate 22 and the

25   growing crystal 24 is relieved in amorphous silicon oxide intermediate layer 28.

After strontium titanate layer 24 has been grown to the desired thickness, the monocrystalline strontium titanate is capped by a template layer 30 that is

30   conducive to the subsequent growth of an epitaxial layer of a desired compound semiconductor material 26. For the subsequent growth of a layer 26 of gallium arsenide, the

MBE growth of strontium titanate monocrystalline layer 24 can be capped by terminating the growth with 1-2 monolayers of titanium, 1-2 monolayers of titanium-oxygen or with 1-2 monolayers of strontium-oxygen. Following

5   the formation of this capping layer, arsenic is deposited to form a Ti-As bond, a Ti-O-As bond or a Sr-O-As. Any of these form an appropriate template 30 for deposition and formation of a gallium arsenide monocrystalline layer 26. Following the formation of template 30, gallium is

10 subsequently introduced to the reaction with the arsenic and gallium arsenide 26 forms. Alternatively, gallium can be deposited on the capping layer to form a Sr-O-Ga bond, and arsenic is subsequently introduced with the gallium to form the GaAs.

15 FIG. 5 is a high resolution Transmission Electron Micrograph (TEM) of semiconductor material manufactured in accordance with the present invention. Single crystal SrTiO3 accommodating buffer layer 24 was grown epitaxially on silicon substrate 22. During this growth

20 process, amorphous interfacial layer 28 is formed which relieves strain due to lattice mismatch. GaAs compound semiconductor layer 26 was then grown epitaxially using template layer 30.

FIG. 6 illustrates an x-ray diffraction spectrum

25 taken on a structure including GaAs compound semiconductor layer 26 grown on silicon substrate 22 using accommodating buffer layer 24. The peaks in the spectrum indicate that both the accommodating buffer layer 24 and GaAs compound semiconductor layer 26 are

30 single crystal and (100) orientated.

The structure illustrated in FIG. 2 can be formed by the process discussed above with the addition of an additional buffer layer 32 deposition step. The

additional buffer layer 32 is formed overlying template
layer 30 before the deposition of monocrystalline
compound semiconductor layer 26. If additional buffer
layer 32 is a compound semiconductor superlattice, such a
5   superlattice can be deposited, by MBE for example, on the
template 30 described above. If instead additional
buffer layer 32 is a layer of germanium, the process
above is modified to cap strontium titanate
monocrystalline layer 24 with a final layer of either
10 strontium or titanium and then by depositing germanium to
react with the strontium or titanium. The germanium
buffer layer 32 can then be deposited directly on this
template 30.

Structure 34, illustrated in FIG. 3, may be formed
15 by growing an accommodating buffer layer, forming an
amorphous oxide layer over substrate 22, and growing
semiconductor layer 38 over the accommodating buffer
layer, as described above. The accommodating buffer
layer and the amorphous oxide layer are then exposed to
20 an anneal process sufficient to change the crystalline
structure of the accommodating buffer layer from
monocrystalline to amorphous, thereby forming an
amorphous layer such that the combination of the
amorphous oxide layer and the now amorphous accommodating
25 buffer layer form a single amorphous oxide layer 36.
Layer 26 is then subsequently grown over layer 38.
Alternatively, the anneal process may be carried out
subsequent to growth of layer 26.

In accordance with one aspect of this embodiment,
30 layer 36 is formed by exposing substrate 22, the
accommodating buffer layer, the amorphous oxide layer,
and semiconductor layer 38 to a rapid thermal anneal
process with a peak temperature of about 700°C to about

1000°C and a process time of about 1 to about 10 minutes. However, other suitable anneal processes may be employed to convert the accommodating buffer layer to an amorphous layer in accordance with the present invention. For

5　example, laser annealing or "conventional" thermal annealing processes (in the proper environment) may be used to form layer 36. When conventional thermal annealing is employed to form layer 36, an overpressure of one or more constituents of layer 30 may be required

10　to prevent degradation of layer 38 during the anneal process. For example, when layer 38 includes GaAs, the anneal environment preferably includes an overpressure of arsenic to mitigate degradation of layer 38.

　　　　As noted above, layer 38 of structure 34 may include

15　any materials suitable for either of layers 32 or 26. Accordingly, any deposition or growth methods described in connection with either layer 32 or 26, may be employed to deposit layer 38.

　　　　FIG. 7 is a high resolution Transmission Electron

20　Micrograph (TEM) of semiconductor material manufactured in accordance with the embodiment of the invention illustrated in FIG. 3. In accordance with this embodiment, a single crystal SrTiO3 accommodating buffer layer was grown epitaxially on silicon substrate 22.

25　During this growth process, an amorphous interfacial layer forms as described above. Next, GaAs layer 38 is formed above the accommodating buffer layer and the accommodating buffer layer is exposed to an anneal process to form amorphous oxide layer 36.

30　　　　FIG. 8 illustrates an x-ray diffraction spectrum taken on a structure including GaAs compound semiconductor layer 38 and amorphous oxide layer 36 formed on silicon substrate 22. The peaks in the

spectrum indicate that GaAs compound semiconductor layer 38 is single crystal and (100) orientated and the lack of peaks around 40 to 50 degrees indicates that layer 36 is amorphous.

The process described above illustrates a process for forming a semiconductor structure including a silicon substrate 22, an overlying oxide layer, and a monocrystalline gallium arsenide compound semiconductor layer 26 by the process of molecular beam epitaxy. The process can also be carried out by the process of chemical vapor deposition (CVD), metal organic chemical vapor deposition (MOCVD), migration enhanced epitaxy (MEE), atomic layer epitaxy (ALE), physical vapor deposition (PVD), chemical solution deposition (CSD), pulsed laser deposition (PLD), or the like. Further, by a similar process, other monocrystalline accommodating buffer layers 24 such as alkaline earth metal titanates, zirconates, hafnates, tantalates, vanadates, ruthenates, and niobates, alkaline earth metal tin-based perovskites, lanthanum aluminate, lanthanum scandium oxide, and gadolinium oxide can also be grown. Further, by a similar process such as MBE, other III-V and II-VI monocrystalline compound semiconductor layers 26 can be deposited overlying monocrystalline oxide accommodating buffer layer 24.

Each of the variations of compound semiconductor materials 26 and monocrystalline oxide accommodating buffer layer 24 uses an appropriate template 30 for initiating the growth of the compound semiconductor layer. For example, if accommodating buffer layer 24 is an alkaline earth metal zirconate, the oxide can be capped by a thin layer of zirconium. The deposition of zirconium can be followed by the deposition of arsenic or

phosphorus to react with the zirconium as a precursor to depositing indium gallium arsenide, indium aluminum arsenide, or indium phosphide respectively. Similarly, if monocrystalline oxide accommodating buffer layer 24 is

5 an alkaline earth metal hafnate, the oxide layer can be capped by a thin layer of hafnium. The deposition of hafnium is followed by the deposition of arsenic or phosphorous to react with the hafnium as a precursor to the growth of an indium gallium arsenide, indium aluminum

10 arsenide, or indium phosphide layer 26, respectively. In a similar manner, strontium titanate 24 can be capped with a layer of strontium or strontium and oxygen, and barium titanate 24 can be capped with a layer of barium or barium and oxygen. Each of these depositions can be

15 followed by the deposition of arsenic or phosphorus to react with the capping material to form a template 30 for the deposition of a compound semiconductor material layer 26 comprising indium gallium arsenide, indium aluminum arsenide, or indium phosphide.

20 The formation of a device structure in accordance with another embodiment of the invention is illustrated schematically in cross-section in FIGs. 9-12. Like the previously described embodiments referred to in FIGs. 1-3, this embodiment of the invention involves the process

25 of forming a compliant substrate utilizing the epitaxial growth of single crystal oxides, such as the formation of accommodating buffer layer 24 previously described with reference to FIGs. 1 and 2 and amorphous layer 36 previously described with reference to FIG. 3, and the

30 formation of a template layer 30. However, the embodiment illustrated in FIGs. 9-12 utilizes a template that includes a surfactant to facilitate layer-by-layer monocrystalline material growth.

Turning now to FIG. 9, an amorphous intermediate layer 58 is grown on substrate 52 at the interface between substrate 52 and a growing accommodating buffer layer 54, which is preferably a monocrystalline crystal

5 oxide layer, by the oxidation of substrate 52 during the growth of layer 54. Layer 54 is preferably a monocrystalline oxide material such as a monocrystalline layer of $Sr_zBa_{1-z}TiO_3$ where z ranges from 0 to 1. However, layer 54 may also comprise any of those compounds

10 previously described with reference to layer 24 in FIGs. 1-2 and any of those compounds previously described with reference to layer 36 in FIG. 3 which is formed from layers 24 and 28 referenced in FIGs. 1 and 2.

Layer 54 is grown with a strontium (Sr) terminated

15 surface represented in FIG. 9 by hatched line 55 which is followed by the addition of a template layer 60 which includes a surfactant layer 61 and capping layer 63 as illustrated in FIGs. 10 and 11. Surfactant layer 61 may comprise, but is not limited to, elements such as Al, In

20 and Ga, but will be dependent upon the composition of layer 54 and the overlying layer of monocrystalline material for optimal results. In one exemplary embodiment, aluminum (Al) is used for surfactant layer 61 and functions to modify the surface and surface energy of

25 layer 54. Preferably, surfactant layer 61 is epitaxially grown, to a thickness of one to two monolayers, over layer 54 as illustrated in FIG. 10 by way of molecular beam epitaxy (MBE), although other epitaxial processes may also be performed including chemical vapor deposition

30 (CVD), metal organic chemical vapor deposition (MOCVD), migration enhanced epitaxy (MEE), atomic layer epitaxy (ALE), physical vapor deposition (PVD), chemical solution

deposition (CSD), pulsed laser deposition (PLD), or the like.

Surfactant layer 61 is then exposed to a Group V element such as arsenic, for example, to form capping layer 63 as illustrated in FIG. 11. Surfactant layer 61 may be exposed to a number of materials to create capping layer 63 such as elements which include, but are not limited to, As, P, Sb and N. Surfactant layer 61 and capping layer 63 combine to form template layer 60.

Monocrystalline material layer 66, which in this example is a compound semiconductor such as GaAs, is then deposited via MBE, CVD, MOCVD, MEE, ALE, PVD, CSD, PLD, or the like to form the final structure illustrated in FIG. 12.

FIGs. 13-16 illustrate possible molecular bond structures for a specific example of a compound semiconductor structure formed in accordance with the embodiment of the invention illustrated in FIGs. 9-12. More specifically, FIGs. 13-16 illustrate the growth of GaAs (layer 66) on the strontium terminated surface of a strontium titanate monocrystalline oxide (layer 54) using a surfactant containing template (layer 60).

The growth of a monocrystalline material layer 66 such as GaAs on an accommodating buffer layer 54 such as a strontium titanium oxide over amorphous interface layer 58 and substrate layer 52, both of which may comprise materials previously described with reference to layers 28 and 22, respectively in FIGs. 1 and 2, illustrates a critical thickness of about 1000 Angstroms where the two-dimensional (2D) and three-dimensional (3D) growth shifts because of the surface energies involved. In order to maintain a true layer by layer growth (Frank Van der Mere growth), the following relationship must be satisfied:

$$\delta_{STO} > (\delta_{INT} + \delta_{GaAs})$$

where the surface energy of the monocrystalline

5   oxide layer 54 must be greater than the surface energy of

the amorphous interface layer 58 added to the surface

energy of the GaAs layer 66. Since it is impracticable

to satisfy this equation, a surfactant containing

template was used, as described above with reference to

10   FIGs. 10-12, to increase the surface energy of the

monocrystalline oxide layer 54 and also to shift the

crystalline structure of the template to a diamond-like

structure that is in compliance with the original GaAs

layer.

15   FIG. 13 illustrates the molecular bond structure of

a strontium terminated surface of a strontium titanate

monocrystalline oxide layer. An aluminum surfactant

layer is deposited on top of the strontium terminated

surface and bonds with that surface as illustrated in

20   FIG. 14, which reacts to form a capping layer comprising

a monolayer of Al_2Sr having the molecular bond structure

illustrated in FIG. 14 which forms a diamond-like

structure with an sp^3 hybrid terminated surface that is

compliant with compound semiconductors such as GaAs. The

25   structure is then exposed to As to form a layer of AlAs

as shown in FIG. 15. GaAs is then deposited to complete

the molecular bond structure illustrated in FIG. 16 which

has been obtained by 2D growth. The GaAs can be grown to

any thickness for forming other semiconductor structures,

30   devices, or integrated circuits. Alkaline earth metals

such as those in Group IIA are those elements preferably

used to form the capping surface of the monocrystalline

oxide layer 54 because they are capable of forming a desired molecular structure with aluminum.

In this embodiment, a surfactant containing template layer aids in the formation of a compliant substrate for
5   the monolithic integration of various material layers including those comprised of Group III-V compounds to form high quality semiconductor structures, devices and integrated circuits. For example, a surfactant containing template may be used for the monolithic
10   integration of a monocrystalline material layer such as a layer comprising Germanium (Ge), for example, to form high efficiency photocells.

Turning now to FIGs. 17-20, the formation of a device structure in accordance with still another
15   embodiment of the invention is illustrated in cross-section. This embodiment utilizes the formation of a compliant substrate which relies on the epitaxial growth of single crystal oxides on silicon followed by the epitaxial growth of single crystal silicon onto the
20   oxide.

An accommodating buffer layer 74 such as a monocrystalline oxide layer is first grown on a substrate layer 72, such as silicon, with an amorphous interface layer 78 as illustrated in FIG. 17. Monocrystalline
25   oxide layer 74 may be comprised of any of those materials previously discussed with reference to layer 24 in FIGs. 1 and 2, while amorphous interface layer 78 is preferably comprised of any of those materials previously described with reference to the layer 28 illustrated in FIGs. 1 and
30   2. Substrate 72, although preferably silicon, may also comprise any of those materials previously described with reference to substrate 22 in FIGs. 1-3.

Next, a silicon layer 81 is deposited over monocrystalline oxide layer 74 via MBE, CVD, MOCVD, MEE, ALE, PVD, CSD, PLD, and the like as illustrated in FIG. 18 with a thickness of a few hundred Angstroms but

5   preferably with a thickness of about 50 Angstroms. Monocrystalline oxide layer 74 preferably has a thickness of about 20 to 100 Angstroms.

Rapid thermal annealing is then conducted in the presence of a carbon source such as acetylene or methane,

10   for example at a temperature within a range of about 800°C to 1000°C to form capping layer 82 and silicate amorphous layer 86. However, other suitable carbon sources may be used as long as the rapid thermal annealing step functions to amorphize the monocrystalline oxide layer 74

15   into a silicate amorphous layer 86 and carbonize the top silicon layer 81 to form capping layer 82 which in this example would be a silicon carbide (SiC) layer as illustrated in FIG. 19. The formation of amorphous layer 86 is similar to the formation of layer 36 illustrated in

20   FIG. 3 and may comprise any of those materials described with reference to layer 36 in FIG. 3 but the preferable material will be dependent upon the capping layer 82 used for silicon layer 81.

Finally, a compound semiconductor layer 96, shown in

25   FIG. 20, such as gallium nitride (GaN) is grown over the SiC surface by way of MBE, CVD, MOCVD, MEE, ALE, PVD, CSD, PLD, or the like to form a high quality compound semiconductor material for device formation. More specifically, the deposition of GaN and GaN based systems

30   such as GaInN and AlGaN will result in the formation of dislocation nets confined at the silicon/amorphous region. The resulting nitride containing compound

semiconductor material may comprise elements from groups III, IV and V of the periodic table and is defect free.

Although GaN has been grown on SiC substrate in the past, this embodiment of the invention possesses a one step formation of the compliant substrate containing a SiC top surface and an amorphous layer on a Si surface. More specifically, this embodiment of the invention uses an intermediate single crystal oxide layer that is amorphized to form a silicate layer which adsorbs the strain between the layers. Moreover, unlike past use of a SiC substrate, this embodiment of the invention is not limited by wafer size which is usually less than 50 mm in diameter for prior art SiC substrates.

The monolithic integration of nitride containing semiconductor compounds containing group III-V nitrides and silicon devices can be used for high temperature RF applications and optoelectronics. GaN systems have particular use in the photonic industry for the blue/green and UV light sources and detection. High brightness light emitting diodes (LEDs) and lasers may also be formed within the GaN system.

FIGs. 21-23 schematically illustrate, in cross-section, the formation of another embodiment of a device structure in accordance with the invention. This embodiment includes a compliant layer that functions as a transition layer that uses clathrate or Zintl type bonding. More specifically, this embodiment utilizes an intermetallic template layer to reduce the surface energy of the interface between material layers thereby allowing for two-dimensional layer-by-layer growth.

The structure illustrated in FIG. 21 includes a monocrystalline substrate 102, an amorphous interface layer 108 and an accommodating buffer layer 104.

Amorphous interface layer 108 is formed on substrate 102 at the interface between substrate 102 and accommodating buffer layer 104 as previously described with reference to FIGs. 1 and 2. Amorphous interface layer 108 may

5 comprise any of those materials previously described with reference to amorphous interface layer 28 in FIGs. 1 and 2. Substrate 102 is preferably silicon but may also comprise any of those materials previously described with reference to substrate 22 in FIGs. 1-3.

10 A template layer 130 is deposited over accommodating buffer layer 104 as illustrated in FIG. 22 and preferably comprises a thin layer of Zintl type phase material composed of metals and metalloids having a great deal of ionic character. As in previously described embodiments,

15 template layer 130 is deposited by way of MBE, CVD, MOCVD, MEE, ALE, PVD, CSD, PLD, or the like to achieve a thickness of one monolayer. Template layer 130 functions as a "soft" layer with non-directional bonding but high crystallinity which absorbs stress build up between

20 layers having lattice mismatch. Materials for template 130 may include, but are not limited to, materials containing Si, Ga, In, and Sb such as, for example, $AlSr_2$, $(MgCaYb)Ga_2$, $(Ca,Sr,Eu,Yb)In_2$, $BaGe_2As$, and $SrSn_2As_2$.

A monocrystalline material layer 126 is epitaxially

25 grown over template layer 130 to achieve the final structure illustrated in FIG. 23. As a specific example, an $SrAl_2$ layer may be used as template layer 130 and an appropriate monocrystalline material layer 126 such as a compound semiconductor material GaAs is grown over the

30 $SrAl_2$. The Al-Ti (from the accommodating buffer layer of layer of $Sr_zBa_{1-z}TiO_3$ where z ranges from 0 to 1) bond is mostly metallic while the Al-As (from the GaAs layer) bond is weakly covalent. The Sr participates in two

distinct types of bonding with part of its electric charge going to the oxygen atoms in the lower accommodating buffer layer 104 comprising $Sr_zBa_{1-z}TiO_3$ to participate in ionic bonding and the other part of its valence charge being donated to Al in a way that is typically carried out with Zintl phase materials. The amount of the charge transfer depends on the relative electronegativity of elements comprising the template layer 130 as well as on the interatomic distance. In this example, Al assumes an sp^3 hybridization and can readily form bonds with monocrystalline material layer 126, which in this example, comprises compound semiconductor material GaAs.

The compliant substrate produced by use of the Zintl type template layer used in this embodiment can absorb a large strain without a significant energy cost. In the above example, the bond strength of the Al is adjusted by changing the volume of the $SrAl_2$ layer thereby making the device tunable for specific applications which include the monolithic integration of III-V and Si devices and the monolithic integration of high-k dielectric materials for CMOS technology.

Clearly, those embodiments specifically describing structures having compound semiconductor portions and Group IV semiconductor portions, are meant to illustrate embodiments of the present invention and not limit the present invention. There are a multiplicity of other combinations and other embodiments of the present invention. For example, the present invention includes structures and methods for fabricating material layers which form semiconductor structures, devices and integrated circuits including other layers such as metal and non-metal layers. More specifically, the invention

includes structures and methods for forming a compliant
substrate which is used in the fabrication of
semiconductor structures, devices and integrated circuits
and the material layers suitable for fabricating those
5   structures, devices, and integrated circuits. By using
embodiments of the present invention, it is now simpler
to integrate devices that include monocrystalline layers
comprising semiconductor and compound semiconductor
materials as well as other material layers that are used
10   to form those devices with other components that work
better or are easily and/or inexpensively formed within
semiconductor or compound semiconductor materials. This
allows a device to be shrunk, the manufacturing costs to
decrease, and yield and reliability to increase.

15   In accordance with one embodiment of this invention,
a monocrystalline semiconductor or compound semiconductor
wafer can be used in forming monocrystalline material
layers over the wafer. In this manner, the wafer is
essentially a "handle" wafer used during the fabrication
20   of semiconductor electrical components within a
monocrystalline layer overlying the wafer. Therefore,
electrical components can be formed within semiconductor
materials over a wafer of at least approximately 200
millimeters in diameter and possibly at least
25   approximately 300 millimeters.

By the use of this type of substrate, a relatively
inexpensive "handle" wafer overcomes the fragile nature
of compound semiconductor or other monocrystalline
material wafers by placing them over a relatively more
30   durable and easy to fabricate base material. Therefore,
an integrated circuit can be formed such that all
electrical components, and particularly all active
electronic devices, can be formed within or using the

monocrystalline material layer even though the substrate itself may include a monocrystalline semiconductor material. Fabrication costs for compound semiconductor devices and other devices employing non-silicon

5 monocrystalline materials should decrease because larger substrates can be processed more economically and more readily compared to the relatively smaller and more fragile substrates (e.g. conventional compound semiconductor wafers).

10   FIG. 24 illustrates schematically, in cross section, a device structure 50 in accordance with a further embodiment. Device structure 50 includes a monocrystalline semiconductor substrate 52, preferably a monocrystalline silicon wafer. Monocrystalline

15 semiconductor substrate 52 includes two regions, 53 and 57. An electrical semiconductor component generally indicated by the dashed line 56 is formed, at least partially, in region 53. Electrical component 56 can be a resistor, a capacitor, an active semiconductor

20 component such as a diode or a transistor or an integrated circuit such as a CMOS integrated circuit. For example, electrical semiconductor component 56 can be a CMOS integrated circuit configured to perform digital signal processing or another function for which silicon

25 integrated circuits are well suited. The electrical semiconductor component in region 53 can be formed by conventional semiconductor processing as well known and widely practiced in the semiconductor industry. A layer of insulating material 59 such as a layer of silicon

30 dioxide or the like may overlie electrical semiconductor component 56.

        Insulating material 59 and any other layers that may have been formed or deposited during the processing of

semiconductor component 56 in region 53 are removed from the surface of region 57 to provide a bare silicon surface in that region. As is well known, bare silicon surfaces are highly reactive and a native silicon oxide

5 layer can quickly form on the bare surface. A layer of barium or barium and oxygen is deposited onto the native oxide layer on the surface of region 57 and is reacted with the oxidized surface to form a first template layer (not shown). In accordance with one embodiment, a

10 monocrystalline oxide layer is formed overlying the template layer by a process of molecular beam epitaxy. Reactants including barium, titanium and oxygen are deposited onto the template layer to form the monocrystalline oxide layer. Initially during the

15 deposition the partial pressure of oxygen is kept near the minimum necessary to fully react with the barium and titanium to form monocrystalline barium titanate layer. The partial pressure of oxygen is then increased to provide an overpressure of oxygen and to allow oxygen to

20 diffuse through the growing monocrystalline oxide layer. The oxygen diffusing through the barium titanate reacts with silicon at the surface of region 57 to form an amorphous layer of silicon oxide 62 on second region 57 and at the interface between silicon substrate 52 and the

25 monocrystalline oxide layer 65. Layers 65 and 62 may be subject to an annealing process as described above in connection with FIG. 3 to form a single amorphous accommodating layer.

In accordance with an embodiment, the step of

30 depositing the monocrystalline oxide layer 65 is terminated by depositing a second template layer 64, which can be 1-10 monolayers of titanium, barium, barium and oxygen, or titanium and oxygen. A layer 66 of a

monocrystalline compound semiconductor material is then
deposited overlying second template layer 64 by a process
of molecular beam epitaxy. The deposition of layer 66 is
initiated by depositing a layer of arsenic onto template
5   64. This initial step is followed by depositing gallium
and arsenic to form monocrystalline gallium arsenide 66.
Alternatively, strontium can be substituted for barium in
the above example.

In accordance with a further embodiment, a
10   semiconductor component, generally indicated by a dashed
line 68 is formed in compound semiconductor layer 66.
Semiconductor component 68 can be formed by processing
steps conventionally used in the fabrication of gallium
arsenide or other III-V compound semiconductor material
15   devices. Semiconductor component 68 can be any active or
passive component, and preferably is a semiconductor
laser, light emitting diode, photodetector,
heterojunction bipolar transistor (HBT), high frequency
MESFET, or other component that utilizes and takes
20   advantage of the physical properties of compound
semiconductor materials. A metallic conductor
schematically indicated by the line 70 can be formed to
electrically couple device 68 and device 56, thus
implementing an integrated device that includes at least
25   one component formed in silicon substrate 52 and one
device formed in monocrystalline compound semiconductor
material layer 66. Although illustrative structure 50
has been described as a structure formed on a silicon
substrate 52 and having a barium (or strontium) titanate
30   layer 65 and a gallium arsenide layer 66, similar devices
can be fabricated using other substrates, monocrystalline
oxide layers and other compound semiconductor layers as
described elsewhere in this disclosure.

FIG. 25 illustrates a semiconductor structure 71 in accordance with a further embodiment. Structure 71 includes a monocrystalline semiconductor substrate 73 such as a monocrystalline silicon wafer that includes a region 75 and a region 76. An electrical component schematically illustrated by the dashed line 79 is formed in region 75 using conventional silicon device processing techniques commonly used in the semiconductor industry. Using process steps similar to those described above, a monocrystalline oxide layer 80 and an intermediate amorphous silicon oxide layer 83 are formed overlying region 76 of substrate 73. A template layer 84 and subsequently a monocrystalline semiconductor layer 87 are formed overlying monocrystalline oxide layer 80. In accordance with a further embodiment, an additional monocrystalline oxide layer 88 is formed overlying layer 87 by process steps similar to those used to form layer 80, and an additional monocrystalline semiconductor layer 90 is formed overlying monocrystalline oxide layer 88 by process steps similar to those used to form layer 87. In accordance with one embodiment, at least one of layers 87 and 90 are formed from a compound semiconductor material. Layers 80 and 83 may be subject to an annealing process as described above in connection with FIG. 3 to form a single amorphous accommodating layer.

A semiconductor component generally indicated by a dashed line 92 is formed at least partially in monocrystalline semiconductor layer 87. In accordance with one embodiment, semiconductor component 92 may include a field effect transistor having a gate dielectric formed, in part, by monocrystalline oxide layer 88. In addition, monocrystalline semiconductor layer 90 can be used to implement the gate electrode of

that field effect transistor. In accordance with one embodiment, monocrystalline semiconductor layer 87 is formed from a group III-V compound and semiconductor component 92 is a radio frequency amplifier that takes

5   advantage of the high mobility characteristic of group III-V component materials. In accordance with yet a further embodiment, an electrical interconnection schematically illustrated by the line 94 electrically interconnects component 79 and component 92. Structure

10 71 thus integrates components that take advantage of the unique properties of the two monocrystalline semiconductor materials.

Attention is now directed to a method for forming exemplary portions of illustrative composite

15 semiconductor structures or composite integrated circuits like 50 or 71. In particular, the illustrative composite semiconductor structure or integrated circuit 103 shown in FIGs. 26-30 includes a compound semiconductor portion 1022, a bipolar portion 1024, and a

20 MOS portion 1026. In FIG. 26, a p-type doped, monocrystalline silicon substrate 110 is provided having a compound semiconductor portion 1022, a bipolar portion 1024, and an MOS portion 1026. Within bipolar portion 1024, the monocrystalline silicon substrate 110 is doped

25 to form an N^+ buried region 1102. A lightly p-type doped epitaxial monocrystalline silicon layer 1104 is then formed over the buried region 1102 and the substrate 110. A doping step is then performed to create a lightly n-type doped drift region 1117 above the N^+ buried region

30 1102. The doping step converts the dopant type of the lightly p-type epitaxial layer within a section of the bipolar region 1024 to a lightly n-type monocrystalline silicon region. A field isolation region 1106 is then

formed between the bipolar portion 1024 and the MOS
portion 1026. A gate dielectric layer 1110 is formed
over a portion of the epitaxial layer 1104 within MOS
portion 1026, and the gate electrode 1112 is then formed

5 over the gate dielectric layer 1110. Sidewall spacers
1115 are formed along vertical sides of the gate
electrode 1112 and gate dielectric layer 1110.

A p-type dopant is introduced into the drift region
1117 to form an active or intrinsic base region 1114. An

10 n-type, deep collector region 1108 is then formed within
the bipolar portion 1024 to allow electrical connection
to the buried region 1102. Selective n-type doping is
performed to form N^+ doped regions 1116 and the emitter
region 1120. N^+ doped regions 1116 are formed within

15 layer 1104 along adjacent sides of the gate electrode
1112 and are source, drain, or source/drain regions for
the MOS transistor. The N^+ doped regions 1116 and emitter
region 1120 have a doping concentration of at least 1E19
atoms per cubic centimeter to allow ohmic contacts to be

20 formed. A p-type doped region is formed to create the
inactive or extrinsic base region 1118 which is a P^+ doped
region (doping concentration of at least 1E19 atoms per
cubic centimeter).

In the embodiment described, several processing

25 steps have been performed but are not illustrated or
further described, such as the formation of well regions,
threshold adjusting implants, channel punchthrough
prevention implants, field punchthrough prevention
implants, as well as a variety of masking layers. The

30 formation of the device up to this point in the process
is performed using conventional steps. As illustrated, a
standard N-channel MOS transistor has been formed within
the MOS region 1026, and a vertical NPN bipolar

transistor has been formed within the bipolar portion 1024. As of this point, no circuitry has been formed within the compound semiconductor portion 1022.

All of the layers that have been formed during the

5 processing of the bipolar and MOS portions of the integrated circuit are now removed from the surface of compound semiconductor portion 1022. A bare silicon surface is thus provided for the subsequent processing of this portion, for example in the manner set forth above.

10 An accommodating buffer layer 124 is then formed over the substrate 110 as illustrated in FIG. 27. The accommodating buffer layer will form as a monocrystalline layer over the properly prepared (i.e., having the appropriate template layer) bare silicon surface in

15 portion 1022. The portion of layer 124 that forms over portions 1024 and 1026, however, may be polycrystalline or amorphous because it is formed over a material that is not monocrystalline, and therefore, does not nucleate monocrystalline growth. The accommodating buffer layer

20 124 typically is a monocrystalline metal oxide or nitride layer and typically has a thickness in a range of approximately 2-100 nanometers. In one particular embodiment, the accommodating buffer layer is approximately 5-15 nm thick. During the formation of the

25 accommodating buffer layer, an amorphous intermediate layer 122 is formed along the uppermost silicon surfaces of the integrated circuit 103. This amorphous intermediate layer 122 typically includes an oxide of silicon and has a thickness and range of approximately 1-

30 5 nm. In one particular embodiment, the thickness is approximately 2 nm. Following the formation of the accommodating buffer layer 124 and the amorphous intermediate layer 122, a template layer 125 is then

formed and has a thickness in a range of approximately one to ten monolayers of a material. In one particular embodiment, the material includes titanium-arsenic, strontium-oxygen-arsenic, or other similar materials as previously described with respect to FIGS. 1-5. Layers 122 and 124 may be subject to an annealing process as described above in connection with FIG. 3 to form a single amorphous accommodating layer.

A monocrystalline compound semiconductor layer 132 is then epitaxially grown overlying the monocrystalline portion of accommodating buffer layer 124 (or over the amorphous accommodating layer if the annealing process described above has been carried out) as shown in FIG. 28. The portion of layer 132 that is grown over portions of layer 124 that are not monocrystalline may be polycrystalline or amorphous. The monocrystalline compound semiconductor layer can be formed by a number of methods and typically includes a material such as gallium arsenide, aluminum gallium arsenide, indium phosphide, or other compound semiconductor materials as previously mentioned. The thickness of the layer is in a range of approximately 1-5,000 nm, and more preferably 100-500 nm. In this particular embodiment, each of the elements within the template layer are also present in the accommodating buffer layer 124, the monocrystalline compound semiconductor material 132, or both. Therefore, the delineation between the template layer 125 and its two immediately adjacent layers disappears during processing. Therefore, when a transmission electron microscopy (TEM) photograph is taken, an interface between the accommodating buffer layer 124 and the monocrystalline compound semiconductor layer 132 is seen.

At this point in time, sections of the compound
semiconductor layer 132 and the accommodating buffer
layer 124 (or of the amorphous accommodating layer if the
annealing process described above has been carried out)
are removed from portions overlying the bipolar portion
1024 and the MOS portion 1026 as shown in FIG. 29. After
the section is removed, an insulating layer 142 is then
formed over the substrate 110. The insulating layer 142
can include a number of materials such as oxides,
nitrides, oxynitrides, low-k dielectrics, or the like.
As used herein, low-k is a material having a dielectric
constant no higher than approximately 3.5. After the
insulating layer 142 has been deposited, it is then
polished, removing portions of the insulating layer 142
that overlie monocrystalline compound semiconductor layer
132.

A transistor 144 is then formed within the
monocrystalline compound semiconductor portion 1022. A
gate electrode 148 is then formed on the monocrystalline
compound semiconductor layer 132. Doped regions 146 are
then formed within the monocrystalline compound
semiconductor layer 132. In this embodiment, the
transistor 144 is a metal-semiconductor field-effect
transistor (MESFET). If the MESFET is an n-type MESFET,
the doped regions 146 and monocrystalline compound
semiconductor layer 132 are also n-type doped. If a p-
type MESFET were to be formed, then the doped regions 146
and monocrystalline compound semiconductor layer 132
would have just the opposite doping type. The heavier
doped (N^+) regions 146 allow ohmic contacts to be made to
the monocrystalline compound semiconductor layer 132. At
this point in time, the active devices within the
integrated circuit have been formed. This particular

embodiment includes an n-type MESFET, a vertical NPN
bipolar transistor, and a planar n-channel MOS
transistor. Many other types of transistors, including
P-channel MOS transistors, p-type vertical bipolar

5   transistors, p-type MESFETs, and combinations of vertical
and planar transistors, can be used. Also, other
electrical components, such as resistors, capacitors,
diodes, and the like, may be formed in one or more of the
portions 1022, 1024, and 1026.

10   Processing continues to form a substantially
completed integrated circuit 103 as illustrated in FIG.
30. An insulating layer 152 is formed over the
substrate 110. The insulating layer 152 may include an
etch-stop or polish-stop region that is not illustrated

15   in FIG. 30. A second insulating layer 154 is then formed
over the first insulating layer 152. Portions of layers
154, 152, 142, 124, and 122 are removed to define contact
openings where the devices are to be interconnected.
Interconnect trenches are formed within insulating layer

20   154 to provide the lateral connections between the
contacts. As illustrated in FIG. 30, interconnect 1562
connects a source or drain region of the n-type MESFET
within portion 1022 to the deep collector region 1108 of
the NPN transistor within the bipolar portion 1024. The

25   emitter region 1120 of the NPN transistor is connected to
one of the doped regions 1116 of the n-channel MOS
transistor within the MOS portion 1026. The other doped
region 1116 is electrically connected to other portions
of the integrated circuit that are not shown.

30   A passivation layer 156 is formed over the
interconnects 1562, 1564, and 1566 and insulating layer
154. Other electrical connections are made to the
transistors as illustrated as well as to other electrical

or electronic components within the integrated circuit
103 but are not illustrated in the FIGs. Further,
additional insulating layers and interconnects may be
formed as necessary to form the proper interconnections

5   between the various components within the integrated
circuit 103.

As can be seen from the previous embodiment, active
devices for both compound semiconductor and Group IV
semiconductor materials can be integrated into a single

10   integrated circuit. Because there is some difficulty in
incorporating both bipolar transistors and MOS
transistors within a same integrated circuit, it may be
possible to move some of the components within bipolar
portion into the compound semiconductor portion 1022 or

15   the MOS portion 1024. Therefore, the requirement of
special fabricating steps solely used for making a
bipolar transistor can be eliminated. Therefore, there
would only be a compound semiconductor portion and a MOS
portion to the integrated circuit.

20   In still another embodiment, an integrated circuit
can be formed such that it includes an optical laser in a
compound semiconductor portion and an optical
interconnect (waveguide) to a MOS transistor within a
Group IV semiconductor region of the same integrated

25   circuit. FIGs. 31-37 include illustrations of one
embodiment.

FIG. 31 includes an illustration of a cross-
sectional view of a portion of an integrated circuit 160
that includes a monocrystalline silicon wafer 161. An

30   amorphous intermediate layer 162 and an accommodating
buffer layer 164, similar to those previously described,
have been formed over wafer 161. Layers 162 and 164 may
be subject to an annealing process as described above in

connection with FIG. 3 to form a single amorphous accommodating layer. In this specific embodiment, the layers needed to form the optical laser will be formed first, followed by the layers needed for the MOS

5   transistor. In FIG. 31, the lower mirror layer 166 includes alternating layers of compound semiconductor materials. For example, the first, third, and fifth films within the optical laser may include a material such as gallium arsenide, and the second, fourth, and

10   sixth films within the lower mirror layer 166 may include aluminum gallium arsenide or vice versa. Layer 168 includes the active region that will be used for photon generation. Upper mirror layer 170 is formed in a similar manner to the lower mirror layer 166 and includes

15   alternating films of compound semiconductor materials. In one particular embodiment, the upper mirror layer 170 may be p-type doped compound semiconductor materials, and the lower mirror layer 166 may be n-type doped compound semiconductor materials.

20   Another accommodating buffer layer 172, similar to the accommodating buffer layer 164, is formed over the upper mirror layer 170. In an alternative embodiment, the accommodating buffer layers 164 and 172 may include different materials. However, their function is

25   essentially the same in that each is used for making a transition between a compound semiconductor layer and a monocrystalline Group IV semiconductor layer. Layer 172 may be subject to an annealing process as described above in connection with FIG. 3 to form an amorphous

30   accommodating layer. A monocrystalline Group IV semiconductor layer 174 is formed over the accommodating buffer layer 172. In one particular embodiment, the monocrystalline Group IV semiconductor layer 174 includes

germanium, silicon germanium, silicon germanium carbide, or the like.

In FIG. 32, the MOS portion is processed to form electrical components within this upper monocrystalline

5   Group IV semiconductor layer 174. As illustrated in FIG. 32, a field isolation region 171 is formed from a portion of layer 174. A gate dielectric layer 173 is formed over the layer 174, and a gate electrode 175 is formed over the gate dielectric layer 173. Doped regions 177 are

10   source, drain, or source/drain regions for the transistor 181, as shown. Sidewall spacers 179 are formed adjacent to the vertical sides of the gate electrode 175. Other components can be made within at least a part of layer 174. These other components include other transistors

15   (n-channel or p-channel), capacitors, transistors, diodes, and the like.

A monocrystalline Group IV semiconductor layer is epitaxially grown over one of the doped regions 177. An upper portion 184 is P+ doped, and a lower portion 182

20   remains substantially intrinsic (undoped) as illustrated in FIG. 32. The layer can be formed using a selective epitaxial process. In one embodiment, an insulating layer (not shown) is formed over the transistor 181 and the field isolation region 171. The insulating layer is

25   patterned to define an opening that exposes one of the doped regions 177. At least initially, the selective epitaxial layer is formed without dopants. The entire selective epitaxial layer may be intrinsic, or a p-type dopant can be added near the end of the formation of the

30   selective epitaxial layer. If the selective epitaxial layer is intrinsic, as formed, a doping step may be formed by implantation or by furnace doping. Regardless how the P+ upper portion 184 is formed, the insulating

layer is then removed to form the resulting structure
shown in FIG. 32.

The next set of steps is performed to define the
optical laser 180 as illustrated in FIG. 33. The field
5   isolation region 171 and the accommodating buffer layer
172 are removed over the compound semiconductor portion
of the integrated circuit. Additional steps are
performed to define the upper mirror layer 170 and active
layer 168 of the optical laser 180. The sides of the
10 upper mirror layer 170 and active layer 168 are
substantially coterminous.

Contacts 186 and 188 are formed for making
electrical contact to the upper mirror layer 170 and the
lower mirror layer 166, respectively, as shown in FIG.
15 33. Contact 186 has an annular shape to allow light
(photons) to pass out of the upper mirror layer 170 into
a subsequently formed optical waveguide.

An insulating layer 190 is then formed and patterned
to define optical openings extending to the contact layer
20 186 and one of the doped regions 177 as shown in FIG. 34.
The insulating material can be any number of different
materials, including an oxide, nitride, oxynitride, low-k
dielectric, or any combination thereof. After defining
the openings 192, a higher refractive index material 202
25 is then formed within the openings to fill them and to
deposit the layer over the insulating layer 190 as
illustrated in FIG. 35. With respect to the higher
refractive index material 202, "higher" is in relation to
the material of the insulating layer 190 (i.e., material
30 202 has a higher refractive index compared to the
insulating layer 190). Optionally, a relatively thin
lower refractive index film (not shown) could be formed
before forming the higher refractive index material 202.

A hard mask layer 204 is then formed over the high refractive index layer 202. Portions of the hard mask layer 204, and high refractive index layer 202 are removed from portions overlying the opening and to areas
5   closer to the sides of FIG. 35.

The balance of the formation of the optical waveguide, which is an optical interconnect, is completed as illustrated in FIG. 36. A deposition procedure (possibly a dep-etch process) is performed to effectively
10 create sidewalls sections 212. In this embodiment, the sidewall sections 212 are made of the same material as material 202. The hard mask layer 204 is then removed, and a low refractive index layer 214 (low relative to material 202 and layer 212) is formed over the higher
15 refractive index material 212 and 202 and exposed portions of the insulating layer 190. The dash lines in FIG. 36 illustrate the border between the high refractive index materials 202 and 212. This designation is used to identify that both are made of the same material but are
20 formed at different times.

Processing is continued to form a substantially completed integrated circuit as illustrated in FIG. 37. A passivation layer 220 is then formed over the optical laser 180 and MOSFET transistor 181. Although not shown,
25 other electrical or optical connections are made to the components within the integrated circuit but are not illustrated in FIG. 37. These interconnects can include other optical waveguides or may include metallic interconnects.

30 In other embodiments, other types of lasers can be formed. For example, another type of laser can emit light (photons) horizontally instead of vertically. If light is emitted horizontally, the MOSFET transistor

could be formed within the substrate 161, and the optical
waveguide would be reconfigured, so that the laser is
properly coupled (optically connected) to the transistor.
In one specific embodiment, the optical waveguide can

5   include at least a portion of the accommodating buffer
layer. Other configurations are possible.

Clearly, these embodiments of integrated circuits
having compound semiconductor portions and Group IV
semiconductor portions, are meant to illustrate what can

10   be done and are not intended to be exhaustive of all
possibilities or to limit what can be done. There is a
multiplicity of other possible combinations and
embodiments. For example, the compound semiconductor
portion may include light emitting diodes,

15   photodetectors, diodes, or the like, and the Group IV
semiconductor can include digital logic, memory arrays,
and most structures that can be formed in conventional
MOS integrated circuits. By using what is shown and
described herein, it is now simpler to integrate devices

20   that work better in compound semiconductor materials with
other components that work better in Group IV
semiconductor materials. This allows a device to be
shrunk, the manufacturing costs to decrease, and yield
and reliability to increase.

25   Although not illustrated, a monocrystalline Group IV
wafer can be used in forming only compound semiconductor
electrical components over the wafer. In this manner,
the wafer is essentially a "handle" wafer used during the
fabrication of the compound semiconductor electrical

30   components within a monocrystalline compound
semiconductor layer overlying the wafer. Therefore,
electrical components can be formed within III-V or II-VI
semiconductor materials over a wafer of at least

approximately 200 millimeters in diameter and possibly at least approximately 300 millimeters.

By the use of this type of substrate, a relatively inexpensive "handle" wafer overcomes the fragile nature of the compound semiconductor wafers by placing them over a relatively more durable and easy to fabricate base material. Therefore, an integrated circuit can be formed such that all electrical components, and particularly all active electronic devices, can be formed within the compound semiconductor material even though the substrate itself may include a Group IV semiconductor material. Fabrication costs for compound semiconductor devices should decrease because larger substrates can be processed more economically and more readily, compared to the relatively smaller and more fragile, conventional compound semiconductor wafers.

A composite integrated circuit may include components that provide electrical isolation when electrical signals are applied to the composite integrated circuit. The composite integrated circuit may include a pair of optical components, such as an optical source component and an optical detector component. An optical source component may be a light generating semiconductor device, such as an optical laser (e.g., the optical laser illustrated in FIG. 33), a photo emitter, a diode, etc. An optical detector component may be a light-sensitive semiconductor junction device, such as a photodetector, a photodiode, a bipolar junction, a transistor, etc.

A composite integrated circuit may include processing circuitry that is formed at least partly in the Group IV semiconductor portion of the composite integrated circuit. The processing circuitry is

configured to communicate with circuitry external to the composite integrated circuit. The processing circuitry may be electronic circuitry, such as a microprocessor, RAM, logic device, decoder, etc.

5   For the processing circuitry to communicate with external electronic circuitry, the composite integrated circuit may be provided with electrical signal connections to the external electronic circuitry. The composite integrated circuit may also have internal optical communications connections for connecting the processing circuitry in the composite integrated circuit to the electrical connections with the external circuitry. Optical components in the composite integrated circuit may provide the optical communications connections which may electrically isolate the electrical signals in the communications connections from the processing circuitry. Together, the electrical and optical communications connections may be for communicating information, such as data, control, timing, etc.

       A pair of optical components (an optical source component and an optical detector component) in the composite integrated circuit may be configured to pass information. Information that is received or transmitted between the optical pair may be from or for the electrical communications connection between the processing circuitry and the external circuitry while providing electrical isolation for the processing circuitry. If desired, a plurality of optical component pairs may be included in the composite integrated circuit for providing a plurality of communications connections and for providing isolation. For example, a composite integrated circuit receiving a plurality of data bits may

include a pair of optical components for communication of each data bit.

In operation, for example, an optical source component in a pair of components may be configured to generate light (e.g., photons) based on receiving electrical signals from an electrical signal connection with the external circuitry. An optical detector component in the pair of components may be optically connected to the source component to generate electrical signals based on detecting light generated by the optical source component. Information that is communicated between the source and detector components may be digital or analog.

If desired the reverse of this configuration may be used. An optical source component that is responsive to the on-board processing circuitry may be coupled to an optical detector component to have the optical source component generate an electrical signal for use in communications with external circuitry. A plurality of such optical component pair structures may be used for providing two-way connections. In some applications where synchronization is desired, a first pair of optical components may be coupled to provide data communications and a second pair may be coupled for communications synchronization information.

For clarity and brevity, optical detector components that are discussed below are discussed primarily in the context of optical detector components that have been formed in a compound semiconductor portion of a composite integrated circuit. In application, the optical detector component may be formed in many suitable ways (e.g., formed from silicon, etc.).

A composite integrated circuit will typically have
an electric connection for a power supply and a ground
connection. The power and ground connections are in
addition to the communications connections that are
5   discussed above. Processing circuitry in a composite
integrated circuit may include electrically isolated
communications connections and include electrical
connections for power and ground. In most known
applications, power supply and ground connections are
10   usually well-protected by circuitry to prevent harmful
external signals from reaching the composite integrated
circuit. A communications ground may be isolated from
the ground signal in communications connections that use
a ground communications signal.

15   In accordance with the present invention, composite
semiconductor structures as described above may be
provided with optical testing structures.

As shown in FIGs. 38-45, a semiconductor structure
or integrated circuit is formed having regions of
20   different types of semiconductor materials, including a
monocrystalline noncompound semiconductor material and a
monocrystalline compound semiconductor material. The
noncompound semiconductor material typically will include
whatever functional circuitry is desired for the intended
25   use of the structure or device, along with one or more
testing structures or circuits, such as scan chains, for
testing purposes as described above. The compound
semiconductor material may also have functional circuitry
and one or more scan chains, but also preferably has
30   optical coupling elements, as discussed in more detail
below, to allow scan chains on the device--preferably
without regard to whether the scan chain elements are in
the compound semiconductor material or the noncompound

semiconductor material--to communicate optically with
test equipment for inputting the scan signals and reading
the scan chain outputs. As examples, the noncompound
semiconductor portions may be silicon, while the compound
5   semiconductor portions may be GaAs.

The different regions of different types of
semiconductor materials can be provided by starting with
a substrate of one of the materials, and depositing the
other material or materials in the manner discussed above
10   over portions of the substrate, leaving other portions of
the substrate exposed. Thus, in a preferred embodiment
the substrate could be silicon and a compound
semiconductor material such as GaAs can be deposited, as
described above in connection with FIGs. 24 and 25, over
15   only portions of the silicon. Functional circuitry can
then be provided in both the GaAs and the exposed areas
of silicon. The circuitry in the two portions can be
connected by appropriate metallization as described
above.

20   Alternatively, one or more additional semiconductor
materials can be deposited on the substrate semiconductor
material in the form of flush islands as described in co-
pending United States patent application No. 09/607,434,
filed June 30, 2000, which is hereby incorporated by
25   reference in its entirety and which is summarized below
for completeness.

Such an embodiment would have both (a) one or more
compound semiconductor portions and (b) at least one
noncompound semiconductor portion such as a
30   monocrystalline silicon portion, as in FIGs. 38-42, but
with the compound semiconductor portions flush with the
surface of the noncompound semiconductor portion.
Although the discussion of this embodiment, which may be

referred to as a "composite" semiconductor, will focus
for convenience on silicon as the noncompound
semiconductor portion, it will be understood that any
noncompound semiconductor portion, such as a different
Group IV semiconductor portion, may also be used.

A cross section of a portion of a preferred
embodiment of a composite semiconductor 500 according to
this embodiment is shown in FIG. 38. As seen in FIG. 38,
composite semiconductor 500 includes a monocrystalline
silicon substrate 501 in which depressions or wells 502
have been formed. Each well 502 is filled with a
compound semiconductor portion, which may be thought of
as an "island" 504 of compound semiconductor in the
noncompound semiconductor, as seen in the plan view of
FIG. 39.

Composite semiconductor 500 may be made by forming
wells 502 in the noncompound--e.g., monocrystalline
silicon--semiconductor substrate 501. Wells 502 may be
formed, e.g., by any well-known etching process including
both wet and dry etching processes, operating on the
silicon or on a layer of oxide grown on the silicon.
While wells 502 may be substantially circular or of other
shapes, they preferably are substantially rectangular as
shown, with dimensions on the order of hundreds of
micrometers on a side, providing an area sufficient to
form a useful amount of circuitry.

After wells 502 have been formed in silicon
substrate 501, the process described above is carried out
to form, preferably, amorphous layer 528, accommodating
buffer layer 524 and template layer 530, respectively
similar to amorphous layer 28, accommodating buffer layer
24 and template layer 30 described above. As above,
amorphous layer 528 and accommodating buffer layer 524

may be annealed to form a single amorphous accommodating layer.

Monocrystalline compound semiconductor layer 526 of, e.g., GaAs, is then grown on template layer 530,

5   resulting in a structure such as that shown in cross section in FIG. 40. GaAs layer 526 substantially follows the contours of monocrystalline silicon substrate 501, including the contours of wells 502.

A polishing step, which can be any conventional

10   semiconductor polishing technique such as chemical/mechanical polishing (CMP), preferably is then used to remove GaAs layer 526, layer 530, layer 524, and layer 528, down to the original surface 503 of substrate 501. The result is the composite structure 500 shown in

15   FIGs. 38 and 39, in which islands 504 of GaAs (or other monocrystalline compound semiconductor) are present in the surface of the noncompound semiconductor substrate 501. Preferably, layer 530, layer 524, and layer 528 (whether annealed or not) or as many of those layers as

20   are present (one or more may be omitted)--which may be referred to collectively as insulating layer 505, insulate the compound semiconductor islands 504 from the noncompound semiconductor 501. If insulating layer 505 does not grow sufficiently on the side walls of wells 502

25   to provide adequate insulation at the edges of island 504, then as shown in FIG. 41 a trench 506 may be cut around the periphery of island 504, using conventional semiconductor trench-forming techniques, and filled with a suitable insulating material 507, which may be, e.g., a

30   silicon oxide, or one of the components of insulating layer 505.

The depth of each well 502, and thus the thickness of each island 504 (the thicknesses of the template layer

530, accommodating buffer layer 524, and amorphous layer 528 total between about 10Å and about 100Å and are therefore negligible), preferably is between about 0.5 μm and about 2 μm.

5   Once composite structure 500 has been formed, electronic circuitry can be created by forming electronic components 556 and 568 in substrate 501 and island(s) 504, respectively. Alternatively, component 556 may be formed in substrate 501 prior to the formation of

10   island(s) 504. Either way, the components can be interconnected by appropriate metallization 570 as shown in FIG. 42, resulting in composite integrated circuit device 515.

       If flush islands are not used, the composite

15   structure may be like that shown above in FIGs. 24 and 25, where the GaAs (or other compound semiconductor material) is formed as a "mesa" on the silicon (or other noncompound semiconductor) substrate, with electronic components 56, 78 and 68, 92 in the compound and

20   noncompound regions, respectively, connected by appropriate metallization 70, 94.

       Whether islands or mesas of the compound semiconductor materials are used, test structures, preferably in the form of scan chains 301, are provided

25   in composite structure 300, as shown in FIG. 43. As depicted in FIG. 43, composite structure 300 has areas 302 of compound semiconductor material on a substrate 303 of noncompound semiconductor material. Scan chains 301 preferably extend throughout structure 300 but each

30   preferably terminates in one of compound semiconductor areas 302, in which is preferably formed an optical element 304 (either a detector or emitter) which can be used, respectively, to input signals to the scan chain or

output signals from the scan chain. In addition, certain
optical elements 305 may be provided to allow observation
of signals at a point or points along a respective scan
chain. As discussed above, compound semiconductor

5   materials are particularly well suited to the formation
of optical elements. The optical detector may be, e.g.,
a photodetector, while the optical emitter may be, e.g.,
a laser or light emitting diode, formed as described
above.

10   For testing composite semiconductor structure 300,
testing equipment 400 (see FIGs. 44 and 45) preferably is
provided with an interface 401 having an arrangement of
optical detectors and emitters complementary to the
arrangement of detectors and emitters on structure 300.

15   Indeed, interface 401 may be another composite structure
like structure 300, conventionally electrically connected
to testing equipment 400.

         In order to test composite structure 300, preferably
the only electrical/mechanical connections that need to

20   be made to structure 300 are to connect power and ground
to two of pads 306, to power the optical coupling
elements 304, 305. Interface 401 of testing equipment
400 preferably is placed opposite structure 300 to be
tested, inputs tests signals optically to the scan

25   chains, and reads the outputs optically. The optical
communications between structure 300 and interface 401
preferably is like the optical communications between two
composite semiconductor structures as described in co-
pending, commonly-assigned United States Patent

30   Application No. 09/607,408, filed June 30, 2000, which is
hereby incorporated by reference in its entirety and
which is summarized as part of the discussion below.

FIGs. 44 and 45 show how composite structure 300 may communicate optically with testing interface 401, and how that communication may be controlled by a third composite semiconductor structure 402.

5   In this particular example, regions 310 and 311 in composite structure 300 and regions 410 and 411 in testing interface 401 may preferably be configured as optical regions. These optical regions, which correspond to particular ones of regions 304, 305 of FIG. 43, may be

10   configured as light-emitting devices, such as a vertical cavity surface emitting laser, another type of suitable laser, or a light-detecting device. The formation of lasers and optical waveguides is described above in more detail in connection with FIGs. 31-37. It is understood

15   that the term "light" as used herein includes infrared, visible and ultraviolet wavelengths of light. Only two optical regions--310, 311 and 410, 411--are shown in each of structure 300 and interface 401 for ease of illustration. It will be understood that the number of

20   optical regions can, and probably will, be greater, as shown in FIG. 43.

As seen in FIG. 44, intermediate structure 402 may be included in testing equipment 400, interposed between composite semiconductor structure 300 to be tested and

25   testing interface 401. Intermediate structure 402, if provided, preferably operates as a filter and/or shutter, preferably including optical regions 420 and 421. Regions 420 and 421 may be configured to be transparent, opaque, or selectively opaque. To selectively limit the

30   light passing through regions 420 and 421, these regions can be implemented using micro-electro-mechanical switches (MEMSs) or piezo-electric devices (either of which may be used, for example, to fully or partially

closes a shutter across the optical region) or a liquid
crystal device. For example, a liquid crystal device can
be used in this fashion to selectively polarize the light
passed through regions 420 and 421.

5   When region 411 is configured as a light-emitting
device, and region 311 is configured as a light-detecting
device, then if region 421 is configured to be
transparent to the particular wavelength of light (it
should be noted that some semiconductor materials are

10   transparent to certain wavelengths of light without
having to remove a portion of the semiconductor),
composite structure 300 and testing interface 401 can
optically communicate with one another. Alternatively,
region 421 can be configured to be opaque, and, thereby,

15   to block communication from region 411 to region 311.

         Similarly, when region 410 is configured as a light-
emitting device and region 310 is configured as a light-
detecting device, region 420 can be configured to be
selectively opaque--i.e., to selectively limit the light

20   detected by region 310. In this manner, intermediate
structure 402 can be used to control the optical
communication between structure 300 and interface 401.

         As shown in FIG. 44, structure 300, intermediate
structure 402 and interface 401 are shown as being

25   vertically stacked--i.e., at least a portion of each of
the circuits is above a portion of another one of the
circuits when the system is oriented in a vertical
direction--with each of structure 300, intermediate
structure 402 and interface 401 preferably defining plane

30   C, B or A, respectively. The planes are preferably
parallel to one another and perpendicular to a single
axis 403. However, the planes may also be oriented at
some angle to one another.

Formation of a region which is transparent--i.e.,
for use in intermediate structure 402--can be
accomplished by substantially removing a portion of the
intermediate structure 402 to form a via--i.e., a free

5   space path. Methods for removal of a portion of the
device are known in the art and include such processes as
chemically etching away or ion-milling the desired
portion of the device. One etching technique, which
would produce angled sidewalls 451 of holes 450 (as shown

10   in FIG. 45) is anisotropic wet etching. Other techniques
for forming holes 450 include reactive ion etching or any
other suitable technique for forming wafer vias or holes.
It should be noted that chemical etching of the strontium
titanate or similar layer may require special etchants as

15   strontium titanate is not etched by common silicon
etchants. Alternatively, the strontium titanate layer
could be used with the common etchants as an etch-stop
layer. Optical signals of a particular wavelength of
light may also be transmitted through solid intervening

20   materials which are transparent to that particular
wavelength.

In the arrangement of FIG. 45, source 452 of
composite structure 300 may transmit light 453 to
detector 454 of testing interface 401 through gap 455 in

25   intermediate structure 402. Gap 455 may extend
completely through intermediate structure 402, or a thin
layer may be left in place as shown in phantom at 456.
Some optical absorption at the wavelength of light 453 by
that thin layer may be acceptable depending on the

30   application. In other cases, a lens or controllable
shutter or filter 457 may be formed above hole or gap
455. As discussed above, shutter or filter 457 may be a
MEMS, piezoelectric or liquid crystal device, or any

other device whose light-transmissive properties can be controlled. Alternatively, in some applications or over some holes or gaps, shutter or filter 457 could be a device whose light-transmissive properties are fixed.

5   Signals from composite testing interface 401 may be transmitted to composite semiconductor structure 300 using source 460. Source 460 may be a downwardly-directed vertical cavity laser diode. Source 460 may transmit test signals as light 461 to detector 462 at the

10   input of a scan chain through gap 463 in the substrate of intermediate structure 402. If gap 463 is covered by a thin layer of semiconductor material as shown in phantom at 464, some optical absorption at the wavelength of light 461 may be acceptable, provided that a sufficiently

15   strong optical signal is transmitted to detector 462. Sources such as sources 452 and 460 may be formed from the compound semiconductor layer. Detectors such as detectors 454 and 462 may be formed from the compound semiconductor layer or from the monocrystalline substrate

20   (depending on the desired wavelength of operation and other considerations).

     In the embodiment of a composite semiconductor structure just described, optical testing structures were provided in the form of interfaces between testing

25   circuits on the composite semiconductor structure and external testing equipment. FIGs. 46 and 47 show further preferred embodiments in which the optical testing structures themselves perform the testing.

     FIG. 46 shows in cross section a composite device

30   600 similar to that of FIG. 12, having monocrystalline noncompound semiconductor substrate 52 (e.g., silicon or another Group IV material) on which is grown an amorphous intermediate layer 58, an accommodating buffer layer 54,

a template layer 60 including a surfactant layer 61 and a
capping layer 63, and finally compound semiconductor
layer 66 (preferably GaAs), all as described in
connection with FIG. 12.

5   As can be seen in FIG. 46, metallization 601 has
been applied to compound semiconductor layer 66 to
connect devices 602 and 603 in compound semiconductor
layer 66, with a thin layer of compound semiconductor 66
under the metallization. While the scan chain technique
10   may be useful to check for processing defects in the
formation of structure 600, it will not show defects in
metallization 601 unless the defects are in the
metallization between devices of the scan chain.
Therefore, if it is desired to check specific
15   metallization areas, another testing technique is
required, and is provided by the embodiment of FIG. 46.

       As seen in FIG. 46, a photodetector element, such as
PIN diode 604, is formed in substrate 52 under the area
of metallization 601 which is desired to be tested. In
20   fact, diode 604 will be formed before metallization 601,
with the foreknowledge that testing in that location will
be desired upon device completion. A light-emitting
element, such as an edge emitting laser 605, is formed in
GaAs layer 66. An optical waveguide 606 is formed above
25   metallization 601 to be tested using, e.g., the
techniques described above in connection with FIG. 36.
Waveguide 606 preferably includes a core 607 of
relatively high refractive index, surrounded by an upper
cladding layer 608 of lower refractive index than core
30   607 and a lower cladding layer 609 of lower refractive
index than core 607. However, the lower cladding layer
609 preferably should be leaky or lossy so that the
optical mode is loosely confined, to allow a measurable

portion of the electric field of the laser light to reach
PIN diode 604 in substrate 52 (assuming metallization 601
is missing) through the thin layer of compound
semiconductor 62 under the metallization and other thin

5   layers 60, 54, 58. The propagation direction of the
laser light is depicted by arrow 610, and curve 611
represents the strength of the electric field mode
profile. Optical power outside the waveguide core 607 is
known as the evanescent field. As shown, at the region

10   of substrate 52 where diode 604 is formed, the evanescent
field, though small, is measurable and may be detected
(in the absence of metallization 601) by detector 604.
In order to achieve the preferred leakiness or lossiness,
lower cladding layer 609 may be made thinner than upper

15   cladding layer 608, or from a material whose refractive
index, while still lower than that of core 607, is closer
to that of core 607 than is the refractive index of upper
cladding layer 608.

     Thus, light emitted by edge emitting laser 605 (or

20   the electric field of that light) will reach
photodetector diode 604 unless metallization 601 is in
the way. Therefore, in order to test whether or not
metallization 601 is connecting devices 602, 603 as
desired, edge emitting laser 605 is energized and the

25   output of photodetector diode 604 is monitored. If there
is no signal, metallization 601 is presumed to be present
and blocking the optical signal, signifying a good
device; if an optical signal is detected by photodiode
604, then it is known that metallization 601 is absent at

30   least in that area.

     Diode 604, laser 605 and waveguide 606 can be formed
wherever on device 600 it is desired to check on the
presence or absence of a specific structure. The outputs

of the various diodes 604 on device 600 can be routed to
one or more input/output pads to be read electrically as
described above in the case of previously known
mechanisms for reading scan chain outputs.

5   Alternatively, each pair of a diode 604 and a laser 605
can be part of a scan chain 607 whose output can be read
either electrically as was previously known, or optically
as described above.

Instead of an edge-emitting laser 605, a vertical

10 cavity surface emitting layer 705 can be provided, as
shown in FIG. 47. In such a case, as seen in FIG. 47,
which is otherwise substantially similar to FIG. 46, a
diffractive optical element 706 is provided below (or
above) laser 705 to diffract the vertically emitted laser

15 light into horizontal waveguide 606. Emitter 605 (FIG.
46) or 705 could alternatively be a light emitting diode.

Although not shown, it should be noted that
alternatively to being formed on top of compound
semiconductor layer 66, metallization 601 could be formed

20 on top of substrate 52. The laser 605 or 705, and
waveguide 606, preferably would still be formed in
compound semiconductor layer 66 which is better suited to
optical devices.

It should be noted also that the composite

25 structures of FIGs. 46 and 47 may be embodied in either a
mesa format or an island format as described above.

In the foregoing specification, the invention has
been described with reference to specific embodiments.
However, one of ordinary skill in the art appreciates

30 that various modifications and changes can be made
without departing from the scope of the present invention
as set forth in the claims below. Accordingly, the
specification and figures are to be regarded in an

illustrative rather than a restrictive sense, and all such modifications are intended to be included within the scope of present invention.

5   Benefits, other advantages, and solutions to problems have been described above with regard to specific embodiments. However, the benefits, advantages, solutions to problems, and any element(s) that may cause any benefit, advantage, or solution to occur or become more pronounced are not to be construed as a critical,
10 required, or essential feature or element of any or all the claims. As used herein, the terms "comprises," "comprising," or any other variation thereof, are intended to cover a non-exclusive inclusion, such that a process, method, article, or apparatus that comprises a
15 list of elements includes not only those elements but may also include other elements not expressly listed or inherent to such process, method, article, or apparatus.

What is claimed is: